EARTH LEAKAGE CURRENT DETECTOR

EARTH LEAKAGE CURRENT DETECTOR IC

BD54123F

●General Description

BD54123F integrates leakage detector and amplifier. Especially, it is suitable for high sensitivity and a high-speed operation use, and since the operating temperature range is wide, it can be used for various uses.

●Key Specifications

- Operating supply voltage range : 12V to 22V
- Operating temperature range : −40°C to +85°C
- Supply current : 330μA(typ.)
- Trip voltage : 4.92mV to 11.06mV
- Output current ability(Ta=−40℃) : −200μA～(min.)

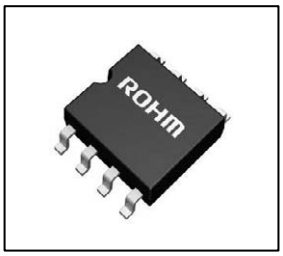
●Features

- Small temperature fluctuation and high input sensitivity
- Wide operating temperature range

●Packages

SOP8

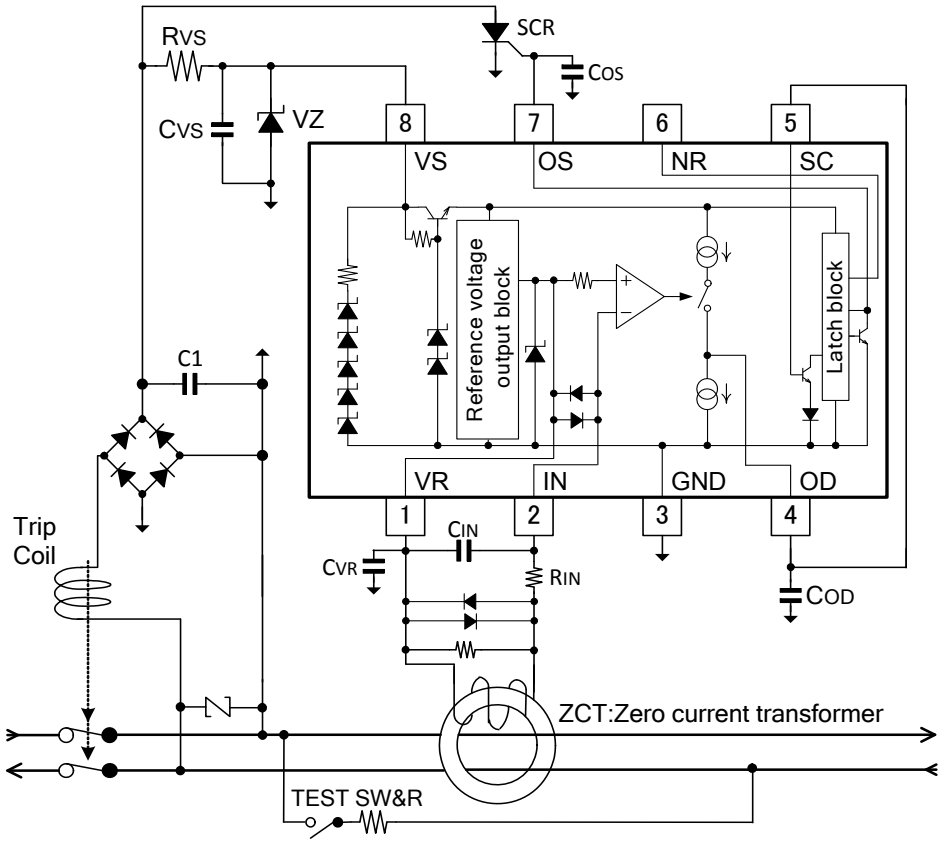
W(Typ.) x D(Typ.) x H(Max.)
5.00mm x 6.20mm x 1.71mm



●Applications

- Earth leakage circuit breaker
- Earth leakage circuit relay

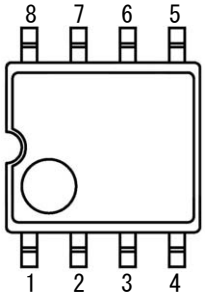
●Typical Application Circuit Example



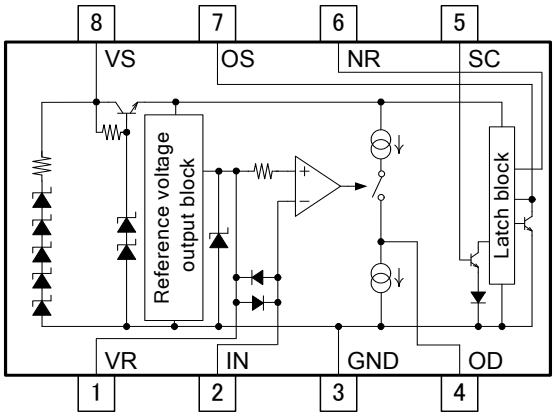
○Product structure : Silicon monolithic integrated circuit ○This product is not designed protection against radioactive rays.

●**Pin Configurations**

SOP8
(TOP VIEW)



●**Block Diagrams**



●**Pin Descriptions**

Pin No.	Symbol	Function
1	VR	Reference voltage
2	IN	Input
3	GND	Ground
4	OD	Output of input comparator
5	SC	Input of latch circuit
6	NR	Noise absorption
7	OS	Output
8	VS	Power supply

●**Absolute Maximum Ratings**

(Ta=25℃)

Parameter	Symbol	Rating	Unit
Supply current *1	IS	8	mA
IN-VR current	I_{IN-VR}	±250	mA
VR pin current	I_{VR}	30	mA
IN terminal current	I_{IN}	30	mA
SC terminal current	I_{SC}	5	mA
Power Supply voltage	VS	36	V
Input terminal voltage	$V_{VR/IN}$	17	V
OD/SC/NR/OS terminal voltage	$V_{OD/SC/NR/OS}$	8	V
Power dissipation	Pd	680 *2	mW
Storage temperature	T_{stg}	−55 to +150	℃

*1 The power-supply voltage is limited by the internal clamping circuit.
*2 To use at temperature above Ta＝25[℃] reduce 5.5mW/℃. Mounted on a glass epoxy PCB (70mm×70mm×1.6mm)

●**Recommended Operating Ratings**

Parameter	Symbol	Limits	Unit
Supply voltage	VS	12 to 22	V
Operating temperature	T_{opr}	−40 to +85	℃
External capacitor between VS and GND	C_{VS}	1≦	μF
External capacitor between OS and GND	C_{OS}	≦1	μF

●**Electrical Characteristics**

(Unless otherwise specified, VS=12V, GND=0V, Ta=25℃)

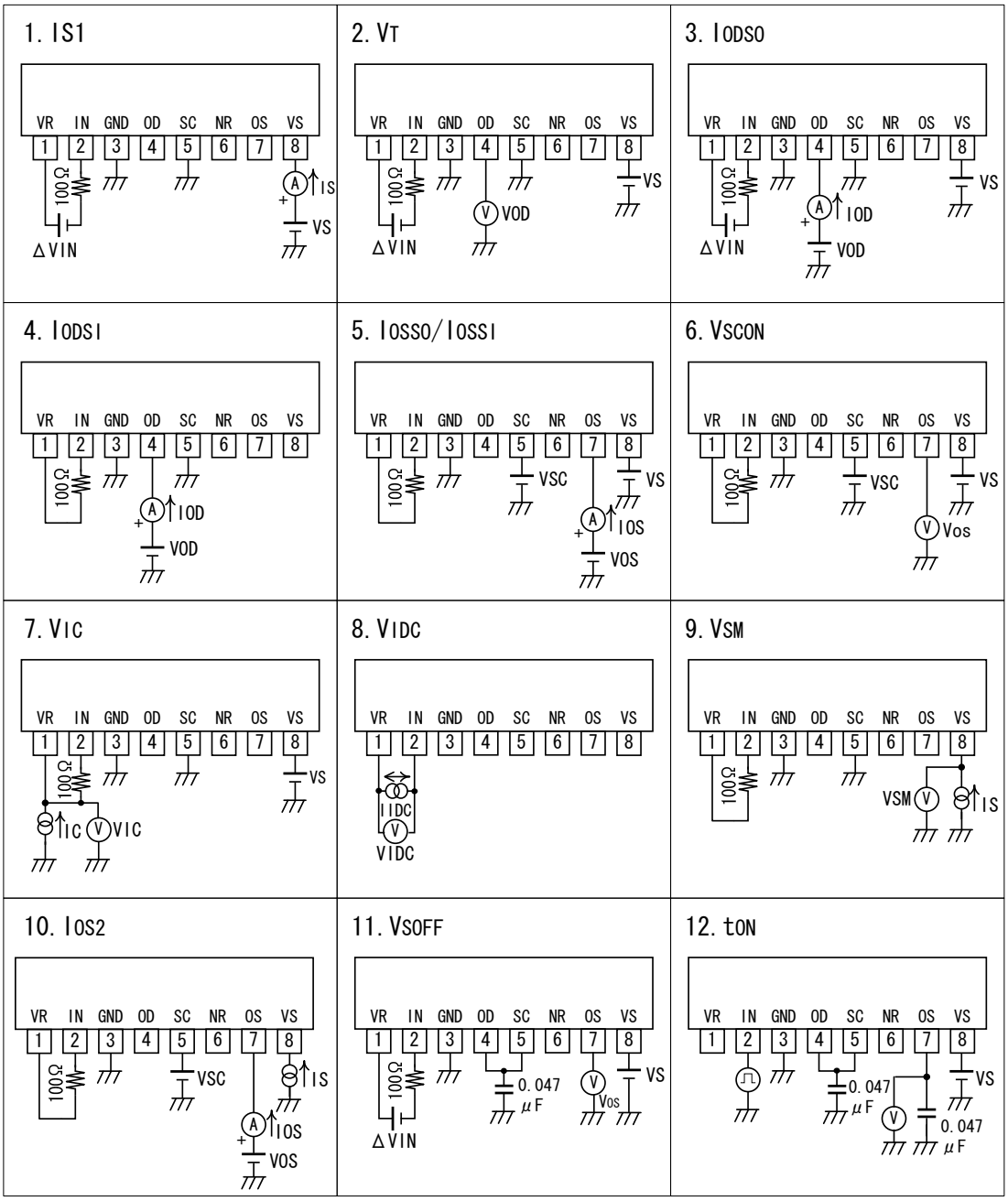
Parameter	Symbol	Temperature range	Limits			Unit	Conditions
			Min.	Typ.	Max.		
Supply current	IS1	-40℃	-	-	520	μA	ΔVIN=V_{VR}-V_{IN}=30mV
		25℃	-	330	500		
		85℃	-	-	460		
Trip voltage	V_T	-40℃ to +85℃	4.92	7.50	11.06	mV	V_T=ΔVIN=V_{VR}-V_{IN}
OD Source current	I_{ODSO}	25℃	-27.2	-20.6	-14.0	μA	ΔVIN=V_{VR}-V_{IN}=30mV, V_{OD}=1.2V
OD Sink current	I_{ODSI}	25℃	16.7	26.0	35.3	μA	V_{OD}=0.8V, ΔVIN=V_{VR}-V_{IN}=0mV
OS Source current	I_{OSSO}	-40℃	-200	-	-	μA	V_{SC}=2.0V, V_{OS}=0.8V
		25℃	-100	-	-		
		85℃	-75	-	-		
OS Sink current	I_{OSSI}	-40℃ to +85℃	200	-	-	μA	V_{SC}=0.2V, V_{OS}=0.2V
SC ON voltage	V_{SCON}	25℃	1.00	1.24	1.48	V	
Input clamp voltage	V_{IC}	-40℃ to +85℃	4.2	5.5	6.7	V	I_{IC}=20mA
Differential input clamp voltage	V_{IDC}	-40℃ to +85℃	0.6	1.0	1.4	V	I_{IDC}=100mA
Maximum current voltage	V_{SM}	25℃	26	29	32	V	IS=7mA
Supply current 2 *1	I_{OS2}	-40℃ to +85℃	-100	-	-	μA	IS=900μA,V_{SC}=2.0V V_{OS}=0.8V
Latch OFF Supply Voltage	V_{SOFF}	25℃	0.5	-	-	V	
Operating time *2	t_{ON}	25℃	1.8	2.9	4.0	ms	

*1 Supply current 2 is OS source current value when the power supply current(Is=900μA) is given.

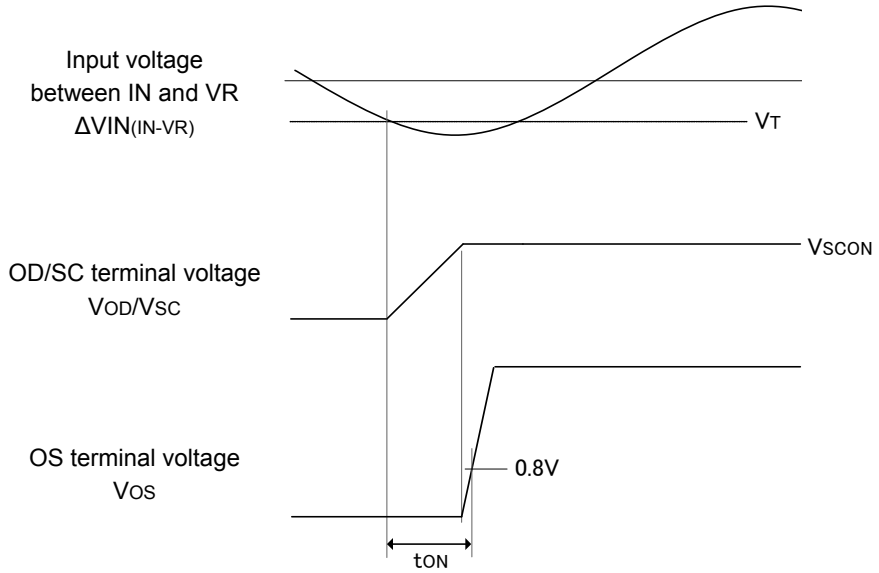
*2 Operating time is time until output voltage reaches 0.8V after detecting the leakage signal.

Conditions : Capacitor(0.047μF) is connected between OD(OS) and GND.

●**Test circuits**



●**Timing Chart**



●**Typical Performance Curves(reference data)**

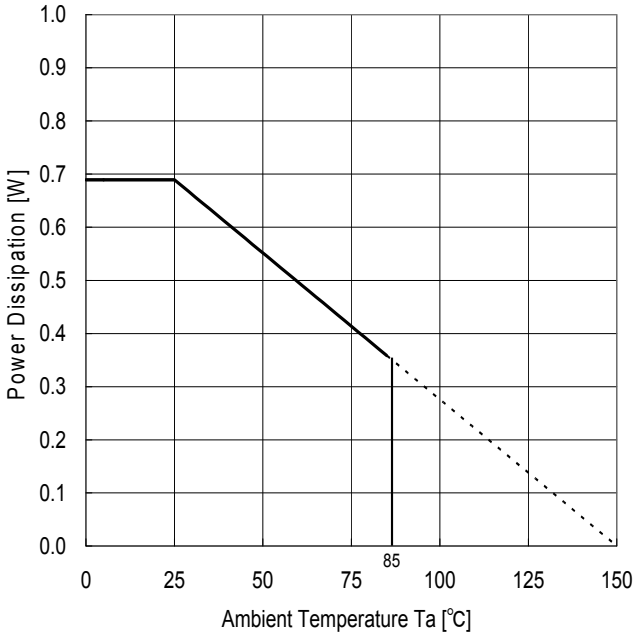


Figure 1
Derating curve

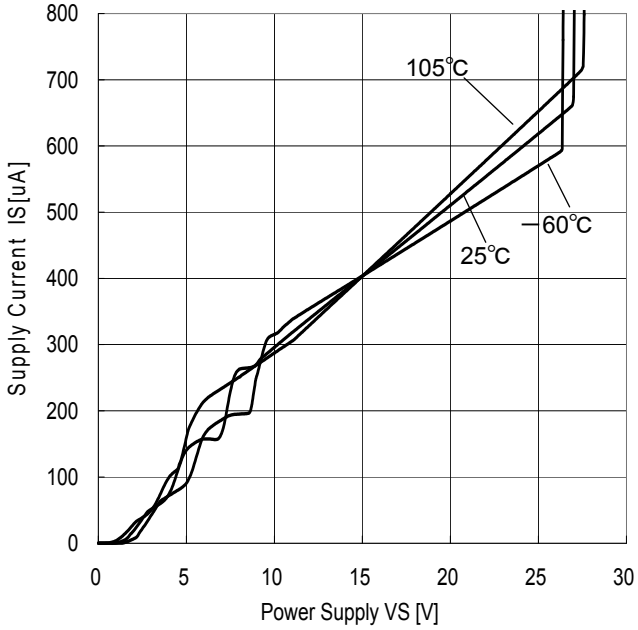


Figure 2
Circuit current - Supply voltage

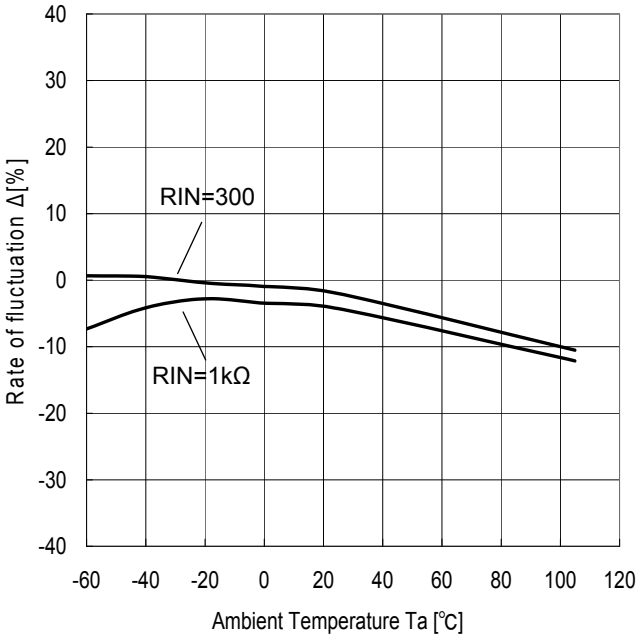


Figure 3
Trip voltage fluctuation rate
- Ambient temperature

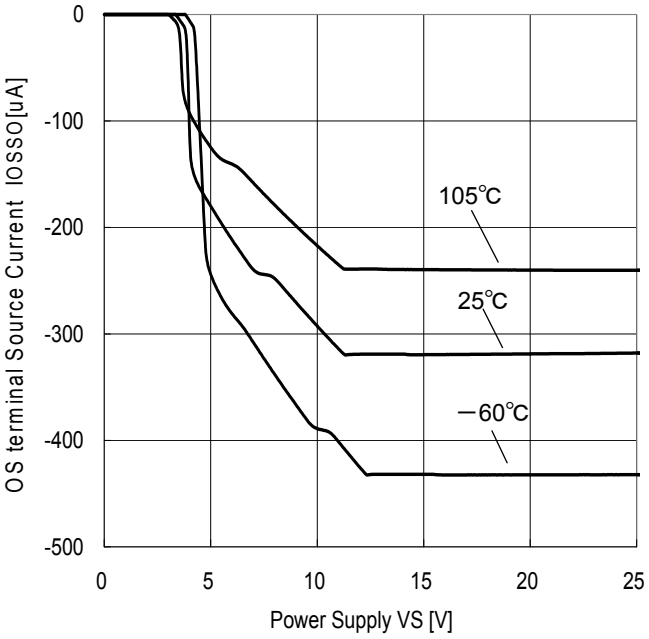


Figure 4
OS terminal source current - Supply voltage

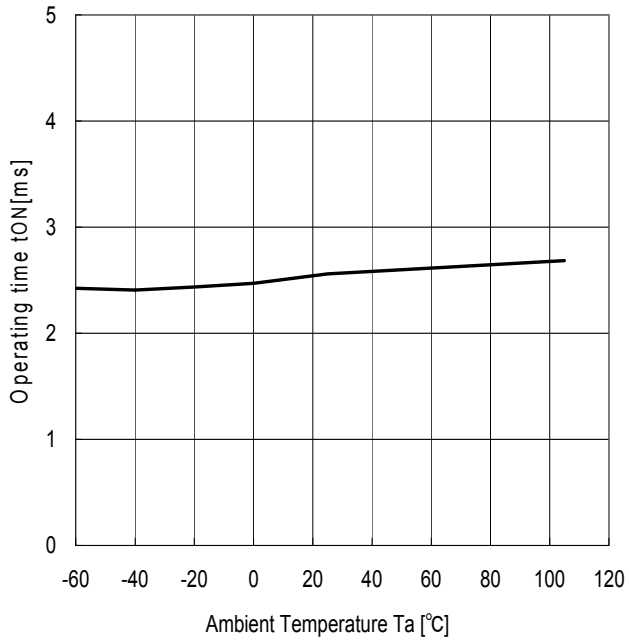


Figure 5
Operating time - Ambient temperature

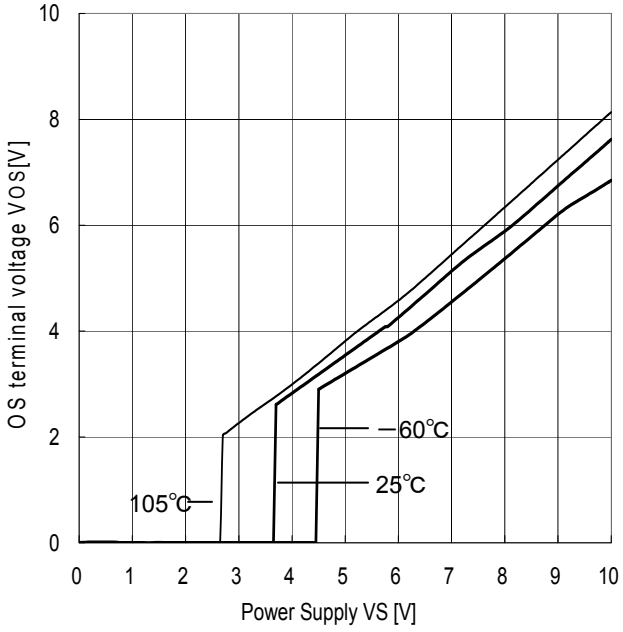


Figure 6
Latch OFF supply voltage - Ambient temperature

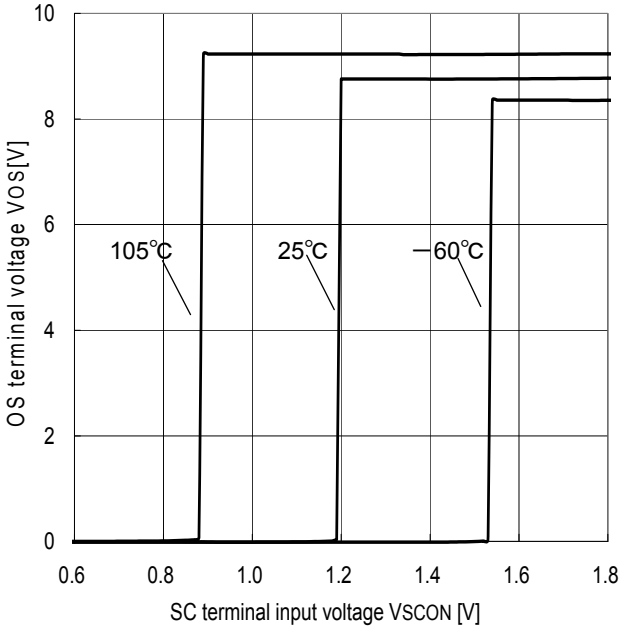


Figure 7
SC ON voltage - Ambient temperature

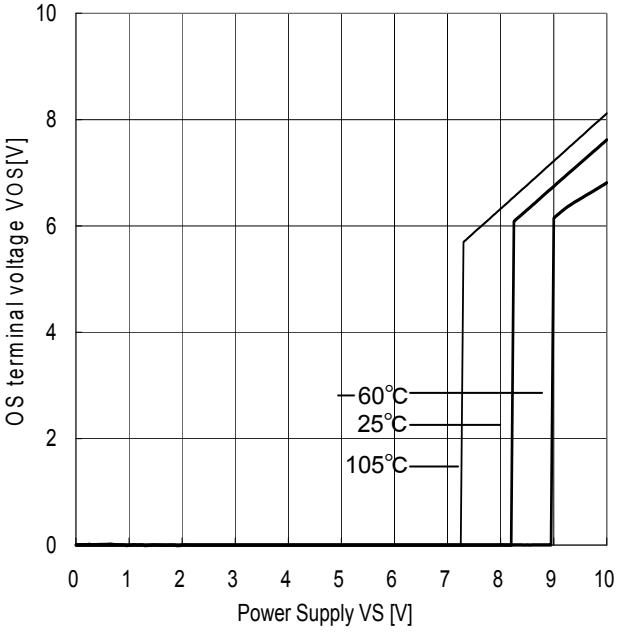


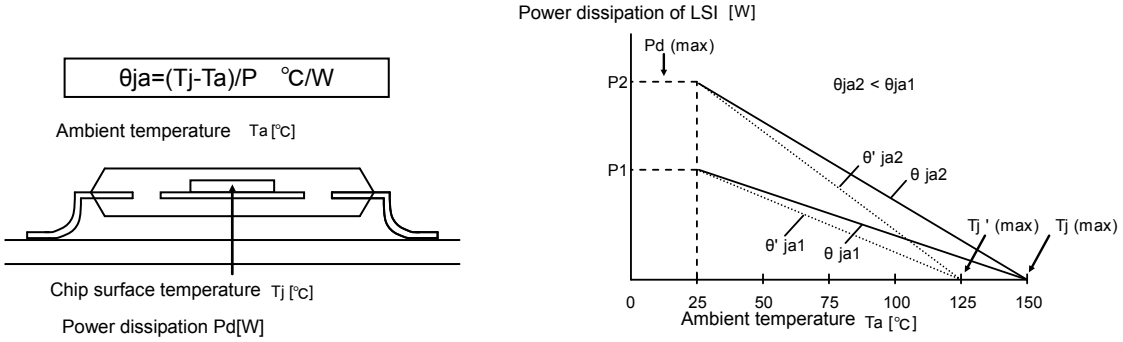
Figure 8
Latch ON supply voltage - Ambient temperature

●Power Dissipation

Power dissipation(total loss) indicates the power that can be consumed by IC at Ta=25℃(normal temperature).IC is heated when it consumed power, and the temperature of IC chip becomes higher than ambient temperature. The temperature that can be accepted by IC chip depends on circuit configuration, manufacturing process, and consumable power is limited. Power dissipation is determined by the temperature allowed in IC chip (maximum junction temperature) and thermal resistance of package (heat dissipation capability). The maximum junction temperature is typically equal to the maximum value in the storage temperature range. Heat generated by consumed power of IC radiates from the mold resin or lead frame of the package. The parameter which indicates this heat dissipation capability(hardness of heat release)is called thermal resistance, represented by the symbol θja℃/W.The temperature of IC inside the package can be estimated by this thermal resistance. Fig.9(a) shows the model of thermal resistance of the package. Thermal resistance θja, ambient temperature Ta, junction temperature Tj, and power dissipation Pd can be calculated by the equation below

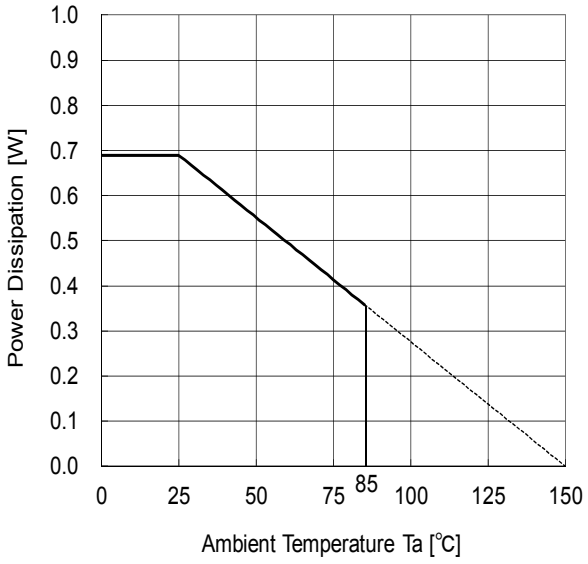
θja = (Tj - Ta) / Pd ℃/W ・・・・・ (Ⅰ)

Derating curve in Fig.9(b) indicates power that can be consumed by IC with reference to ambient temperature. Power that can be consumed by IC begins to attenuate at certain ambient temperature. This gradient is determined by thermal resistance θja. Thermal resistance θja depends on chip size, power consumption, package, ambient temperature, package condition, wind velocity, etc even when the same of package is used. Thermal reduction curve indicates a reference value measured at a specified condition. Fig.10(a) show a derating curve for an example of BD54123F.



(a) Thermal resistance (b) Derating curve

Figure 9. Thermal resistance and derating



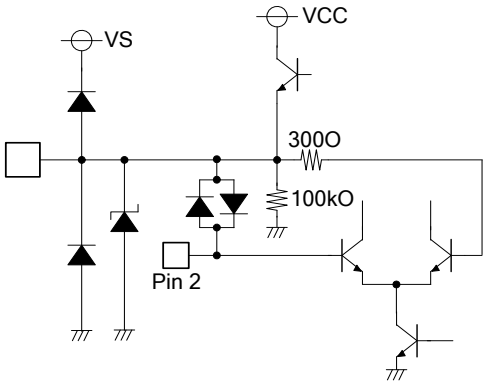
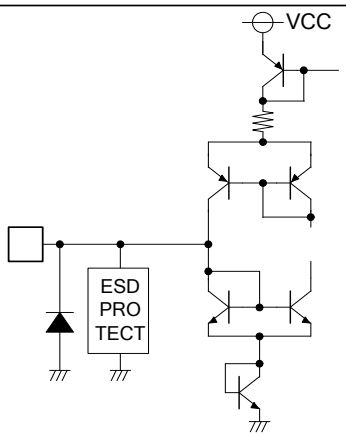
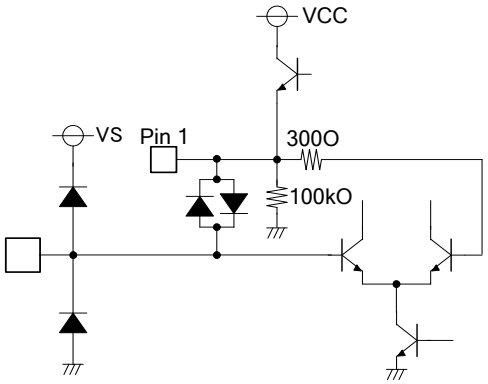
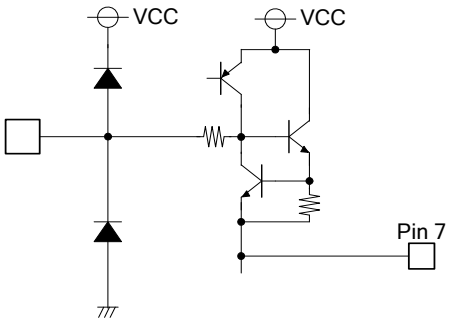
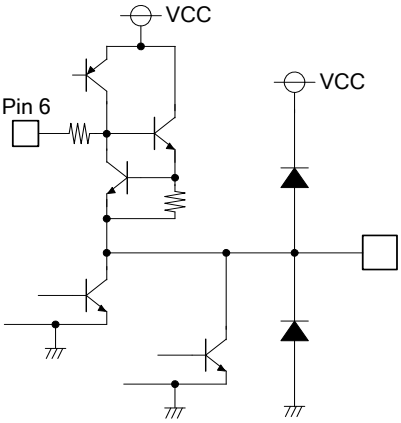
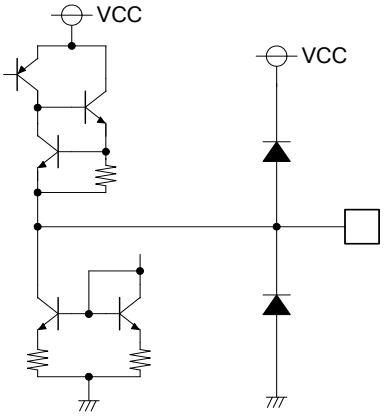
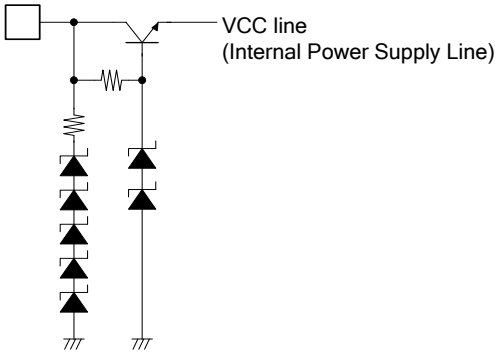
(a) BD54123F

	Derating curve slope	UNIT
BD54123F	5.5	mW/℃

When using the unit above Ta=25℃, subtract the value above per degree℃
Permissible dissipation is a value when FR4 glass epoxy board 70mm×70mm×1.6mm (cooper foil area below 3%) is mounted.

Figure 10. Derating curve

●I/O equivalence circuit

Pin 1 [VR]		Pin 5 [SC]	
Pin 2 [IN]		Pin 6 [NR]	
Pin 3 [GND]		Pin 7 [OS]	
Pin 4 [OD]		Pin 8 [VS]	

●Operational Notes

1) Absolute maximum ratings
Absolute maximum ratings are the values which indicate the limits, within which the given voltage range can be safely charged to the terminal. However, it does not guarantee the circuit operation.

2) Power dissipation Pd
Using the unit in excess of the rated power dissipation may cause deterioration in electrical characteristics due to a rise in chip temperature, including reduced current capability. Therefore, please take into consideration the power dissipation (Pd) under actual operating conditions and apply a sufficient margin in thermal design. Refer to the thermal derating curves for more information.

3) Terminal short-circuits
When the output and power supply terminals are shorted, excessive output current may flow, resulting in undue heat generation and, subsequently, destruction.

4) Ground terminal voltage
All time, Ground terminal voltage should keep lowest voltage.
In addition, please confirm whether there is not really a terminal becoming the voltage that is lower than GND including a transitional phenomenon.

5) Operation in a strong electromagnetic field
Operation in a strong electromagnetic field may cause malfunctions.

6) Short-circuit between pins and erroneous mounting
Incorrect mounting may damage the IC. In addition, the presence of foreign particles between the outputs, the output and the power supply, or the output and GND may result in IC destruction.

7) IC handing
Applying mechanical stress to the IC by deflecting or bending the board may cause fluctuations in the electrical characteristics due to piezo resistance effects.

8) Board inspection
Connecting a capacitor to a pin with low impedance may stress the IC. Therefore, discharging the capacitor after every process is recommended. In addition, when attaching and detaching the jig during the inspection phase, ensure that the power is turned off before inspection and removal. Furthermore, please take measures against ESD in the assembly process as well as during transportation and storage.

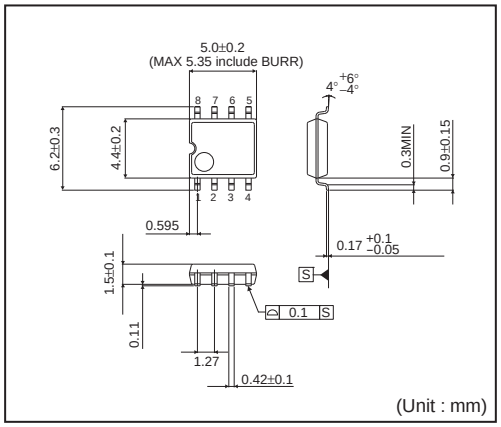
Status of this document
The Japanese version of this document is formal specification. A customer may use this translation version only for a reference to help reading the formal version.
If there are any differences in translation version of this document formal version takes priority.

●Ordering Information

B D 5 4 1 2 3 F	E 2
Part Number	Package F: SOP8
	Packaging and forming specification E2: Embossed tape and reel (SOP8)

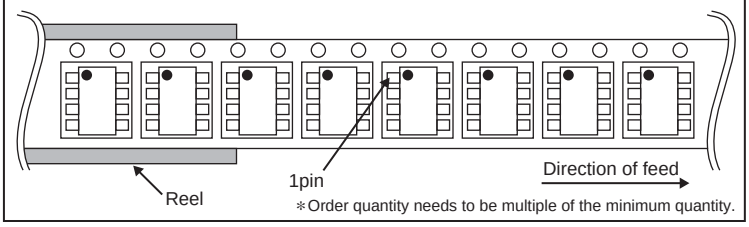
●Physical Dimension Tape and Reel Information

SOP8



<Tape and Reel information>

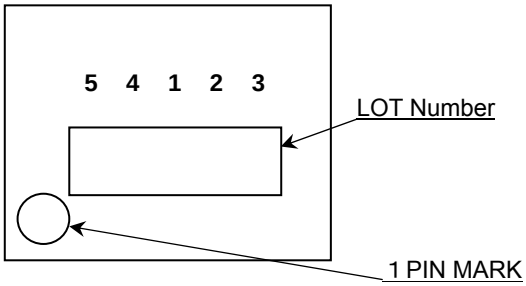
Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

●Marking Diagrams

SOP8
(TOP VIEW)



●**Revision History**

Date	Revision	Changes
2012.10.29	001	New Release